In the Claims:

Kindly amend the claims as indicated.

1. (Currently Amended) A method of testing the routing circuitry in a field programmable gate array (FPGA) having a first FPGA tile, said routing circuitry having a first set of tracks having first and second ends, and a second set of tracks having first and second ends and intersecting said first set of tracks, said second set of tracks used to route the internal signals of the FPGA, said routing structure having programmable interconnect elements at selected intersections of said first set of tracks and said second set of tracks, said method comprising:

defining a set of test inputs for a routed network of a logic circuit;

determining an expected output result for said set of test inputs;

providing a global control signal to said first end of one of said first set and said second set of tracks, said global control signal turns on all interconnect elements of said one of said first set and said second set of tracks simultaneously;

obtaining an actual result by applying said set of test inputs to said routed network, wherein said set of test inputs are applied such that adjacent tracks in said first set of tracks have different logic values and adjacent tracks in said second set of tracks have different logic values;

comparing said expected result with said actual result; and

flagging an error if said expected result is not identical with said actual result;

wherein said first FPGA tile comprises a plurality of interface groups (IGs), each of said IGs having a plurality of input multiplexers configurable to select signals received from outside of said FPGA tile and provide signals to said routing circuitry inside said FPGA tile, and a plurality of input/output pads (I/Os) coupled to at least one of said input multiplexers of at least one of said IGs.

2. (Currently Amended) A method of testing a routing structure in a field programmable gate array (FPGA) having a first FPGA tile, said routing structure having a first set of tracks having first and second ends, and a second set of tracks having first and second ends perpendicular to said first set of tracks, said second set of

tracks used to route the internal signals of the FPGA, said routing structure having programmable interconnect elements at selected ones of said intersections of said first set of tracks and said second set of tracks, said method comprising:

providing a global control signal to said first end of said first set of tracks that turns on all interconnect elements of said first set of tracks simultaneously;

providing a plurality of signal sources to said first end of said first set of tracks, wherein said signal sources are applied to said first end of said first set of tracks such that adjacent tracks in said first set of tracks have different logic values;

providing a circuit at said second end of said first set of tracks, said circuits producing actual output values in response to said plurality of signal sources; and

flagging an error if said actual output values in response to said plurality of signal sources are not identical with expected output values;

wherein said first FPGA tile comprises a plurality of interface groups (IGs), each of said IGs having a plurality of input multiplexers configurable to select signals received from outside of said FPGA tile and provide signals to said routing circuitry inside said FPGA tile, and a plurality of input/output pads (I/Os) coupled to at least one of said input multiplexers of at least one of said IGs.

3. (Currently Amended) A method of testing a routing structure in a~~n~~ field programmable gate array (FPGA) having a first FPGA tile, said routing structure having a first set of tracks having first and second ends and a second set of tracks having first and second ends perpendicular to said first set of tracks, said second set of tracks used to route the internal signals of the FPGA, said routing structure having programmable interconnect elements at selected ones of said intersections of said first set of tracks and said second set of tracks, said method comprising:

providing a global control signal to said first end of said second set of tracks that turns on all interconnect elements of said second set of tracks simultaneously;

providing a plurality of signal sources to said first end of said second set of tracks, wherein said signal sources are applied to said first end of said second set of tracks such that adjacent tracks in said second set of tracks have different logic values;

providing a circuit at said second end of said second set of tracks, said circuits producing actual output values in response to said plurality of signal sources; and

flagging an error if said actual output values in response to said plurality of signal sources are not identical with expected output values;

wherein said first FPGA tile comprises a plurality of interface groups (IGs), each of said IGs having a plurality of input multiplexers configurable to select signals received from outside of said FPGA tile and provide signals to said routing circuitry inside said FPGA tile, and a plurality of input/output pads (I/Os) coupled to at least one of said input multiplexers of at least one of said IGs.

4. (Currently Amended) A method of testing a routing structure in a~~n~~ field programmable gate array (FPGA) having a first FPGA tile, said routing structure having horizontal tracks having first and second ends and vertical tracks having first and second ends used to route the internal signals of the FPGA, said routing structure having programmable interconnect elements at selected ones of said intersections of said horizontal and vertical tracks, said method comprising:

providing a global control signal to said first end of said vertical tracks that turns on all interconnect elements of said vertical tracks simultaneously;

providing a plurality of signal sources to a first end of said vertical tracks, wherein said signal sources are applied to said first end of said vertical tracks such that adjacent tracks in said vertical tracks have different logic values;

providing a NOR circuit and a NAND circuit at said second end of said vertical tracks, said circuits producing actual output values in response to said plurality of signal sources; and

flagging an error if said actual output values in response to said plurality of signal sources are not identical with expected output values;

wherein said first FPGA tile comprises a plurality of interface groups (IGs), each of said IGs having a plurality of input multiplexers configurable to select signals received from outside of said FPGA tile and provide signals to said routing circuitry inside said FPGA tile, and a plurality of input/output pads (I/Os) coupled to at least one of said input multiplexers of at least one of said IGs.

5. (Previously Presented) The method of testing said routing circuitry in an field programmable gate array (FPGA) according to claim 4 wherein the method of testing the routing circuitry further comprises:

providing a global control signal to said first end of said horizontal tracks that turns on all interconnect elements of said horizontal tracks simultaneously;

providing a plurality of signal sources to a first end of said horizontal tracks;

providing a NOR circuit and a NAND circuit at said second end of said horizontal tracks, said circuits producing actual output values; and

flagging an error if said actual output values are not identical with expected output values.